Three-Level Cell Topology for a Multilevel Power Supply to Achieve High Efficiency Envelope Amplifier

Daniel Díaz, Miroslav Vasić, Óscar García, Jesús A. Oliver, Pedro Alou, Roberto Prieto, and José A. Cobos,

Abstract—**This paper presents an envelope amplifier solution for envelope elimination and restoration (EER), that consists of a series combination of a switch-mode power supply (SMPS), based on three-level voltage cells and a linear regulator. This cell topology offers several advantages over a previously presented envelope amplifier based on a different multilevel topology (two-level voltage cells). The topology of the multilevel converter affects to the whole design of the envelope amplifier and a comparison between both design alternatives regarding the size, complexity and the efficiency of the solution is done. Both envelope amplifier solutions have a bandwidth of 2 MHz with an instantaneous maximum power of 50 W. It is also analyzed the linearity of the three-level cell solution, with critical importance in the EER technique implementation. Additionally, considerations to optimize the design of the envelope amplifier and experimental comparison between both cell topologies are included.**

Index Terms—**Envelope amplifier, envelope elimination and restoration (EER), Kahn's technique, multilevel converter, RF power amplifiers, switching capacitors.**

I. Introduction

NOWADAYS, the demand for broadband and wireless services is growing on a daily basis. One of the direct consequences of this development is certainly the growth of the networks that have to provide these services and one of the problems is their energy consumption. Some estimation showed that 1% of the planet's global energy consumption in 2007 was used by telecommunication industry [2]. In [3] it is explained that the efficiency of the first generation of 3G radio base stations is just a few percent and in [4] that the final power amplifier (PA) stage, which consumes most of the power, has a very low efficiency for the transmitted signals.

Poor system efficiency means that significant power is wasted and it requires higher cooling, bigger volume, an increased cost of devices and, in the case that they were battery operated, much shorter autonomy. Having in mind that for the battery operated devices their autonomy is crucial, the problem of a low efficient radio frequency power amplifier (RFPA) gains in importance.

The source of the problem is in the necessity of higher bandwidths and spectral efficiency, due to a communication demand pattern based successively on voice, data and video, having the last one a higher data rate. To cover it, communication schemes have evolved fast. Recent years, communication schemes like code division multiple access (CDMA) (2G), enhanced data rates for GSM evolution (EDGE) (2G-3G) and wireless code division multiple access (WCDMA) (3G) have been used. Nowadays, due to the increase of the video transmissions and to prevent saturation, new broadband standards as worldwide interoperability for microwave access (WiMAX), long term evolution (LTE) and advanced LTE are gaining importance.

To achieve the instantaneous envelope and phase modulation (due to the high spectral efficiency needed), a high linearity is required. This can be achieved with a linear PA, but with a low efficiency (limited to less than 25% for signals with high envelope variations [5] and a fixed supply voltage) due to the high peak to average power ratio (PAPR) signals and to the implementation of the back-off technique. As a result, several techniques have been proposed to increase the efficiency of the radio frequency (RF) amplifier. One alternative is to generate a variable supply voltage for the linear RF power amplifier as in [6] were efficiencies from 42% to 48% can be obtained for an output power in the range of one watt using envelope tracking (ET) technique. In [7], envelope tracking technique is also used with an efficiency of 44% at 25 W, but with a carrier bandwidth limited to 50 kHz.

The efficiency can be increased also using a Doherty amplifier, as in [8], reaching near 50% of efficiency for a power of 50 W and in [9] and [10], where efficiencies of 40.3% and 49.3% have been obtained for an output power of 15.8 W.

Another option is to use a switched PA, with high efficiency, and implement a linearization technique. There are several ways to implement the linearization of a PA, but this work is focused on the Kahn's Technique or Envelope Elimination and Restoration Technique (EER) [11].

The technique called Kahn's Technique or Envelope Elimination and Restoration (EER) Technique is used in order to enhance the efficiency and linearity of the RFPA. The idea of this technique is based on the principle that any narrowband signal can be represented as a simultaneous envelope and phase modulation. In the block diagram presented in Fig. 1 two main parts can be distinguished: the first part serves for the implementation

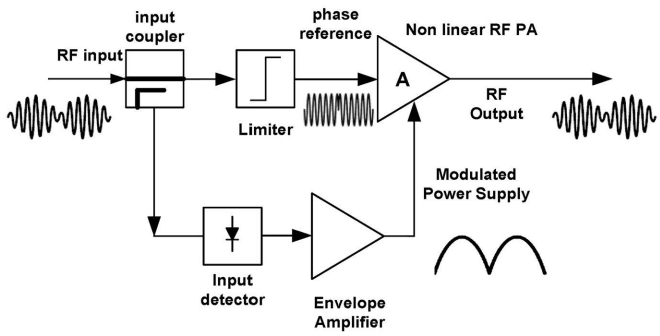


Fig. 1. Block diagram of Kahn's technique.

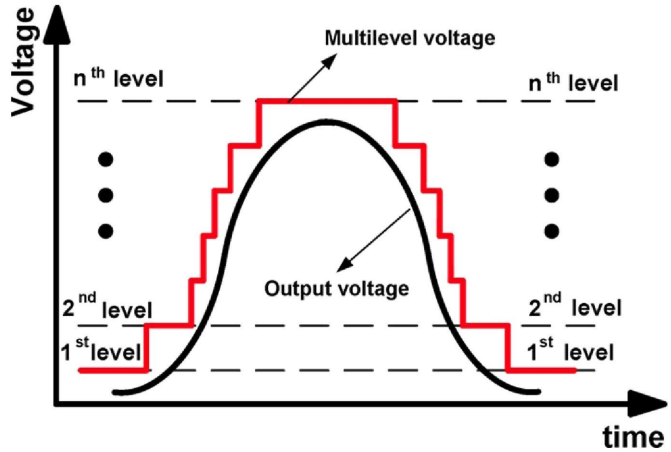


Fig. 2. Main waveforms of the envelope amplifier.

of the envelope modulation, done through the envelope amplifier, while the second one is used for phase modulation. The envelope amplifier varies its output voltage dynamically, being the load a non-linear PA. In this way, the RFPA works as a time domain multiplier, where the envelope modulation is injected to the non-linear PA.

The efficiency of EER technique lies in the high efficiency of the non-linear PAs (theoretically 100% for classes E, D, F) and of their power supply [12]. Non-linear PAs are based on the idea of employing a transistor as a switching device, in a way that the power losses on the transistor are very low, comparing them with the case when it works as a current source in linear classes.

Regarding the envelope amplifier, the aim of this work and one of the key elements of the Kahn-technique transmitter, there are several properties that must be satisfied, such as:

- High linearity
- High efficiency
- Very fast dynamic response
- Minimum interference with the spectrum of the transmitter's output signal

In the state of the art, several solutions for the envelope amplifier can be found, such as a simple buck converter (class S modulator) in [13], [14], a multiphase buck converter in [15], a three level converter in [16] or a linear assisted switching amplifier [17], [18]. These solutions do not exceed the bandwidth of few hundred kHz for power levels above tens of watts [19], not enough for the requirements of the present application (bandwidth in the order of MHz and power about tens of watts). In [20] a buck converter that operates at 130 MHz and has the bandwidth of 15 MHz was integrated on a chip, but the peak power is just 2.2 W while the average power is around 1 W, not sufficient as well for the desired output power.

Since a high efficiency is required by the application, the use of a switched dc-dc converter is mandatory. However, its switching frequency must be at least five times higher than the requested bandwidth (for the bandwidth of 2 MHz it would be necessary to apply a switching frequency of, at least, 10 MHz) [21]. As a result of the increase in the switching frequency, the efficiency of the converter decreases and, as a consequence, the efficiency of the system decreases as well. Conventional solutions for tracking power supplies based only on a switched DC/DC converter [22] neither are a suitable design option for this application because to achieve a high bandwidth (in the range of MHzs) it is not energy efficient to use a DC/DC converter, due to the high switching frequency that has to be used to obtain a high bandwidth.

The solution proposed in this work is based on [23] but using a different topology for the multilevel converter. It consists of a SMPS in series with a linear regulator stage and works in open loop being its maximum switching frequency equal to the maximum frequency of the transmitted envelope (not five times higher).

The implemented envelope amplifier has a bandwidth of 2 MHz for large signal, limited by the speed of the MOSFETs, and up to 5 MHz for small signal, limited by the linear regulator.

Theoretical results in this work are presented for a sinusoidal waveform and for a CDMA signal. To carry out the experimental validation of the system, a sinusoidal waveform of 2 MHz and with a maximum output power of 50 W has been used.

II. Topology of the Envelope Amplifier

In this section the main characteristics of the topology of the envelope amplifier are presented. Special attention is given, at the end of this section, to the operation of the three-level cell, the proposed alternative topology for the multilevel converter.

The envelope amplifier consists of a multilevel converter and a linear regulator in series. The multilevel converter has to supply the linear regulator and it has to provide discrete voltage levels that are as close as possible to the output voltage of the envelope amplifier to increase the efficiency of the converter, while the linear regulator provides a high bandwidth. Main waveforms of the multilevel and linear regulator output voltage are shown in Fig. 2 and in Fig. 3 the block diagram of the solution can be seen.

By modulating the power supply of the linear regulator its efficiency is increased. The dc-dc switching converter operates in open loop and the tight regulation of the output voltage is done by the linear regulator. The main role of the switching converter is to provide the supply voltage to the linear regulator (V_A), which, on the other hand, has to manage all the regulation of the output voltage.

Additionally to the two-stage configuration shown in Fig. 3, the DC-DC converter contains, as explained later in this section, stacked cells or multiplexed voltage inputs. Both design

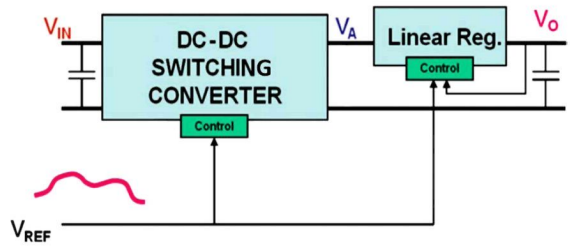


Fig. 3. Block diagram of the proposed system.

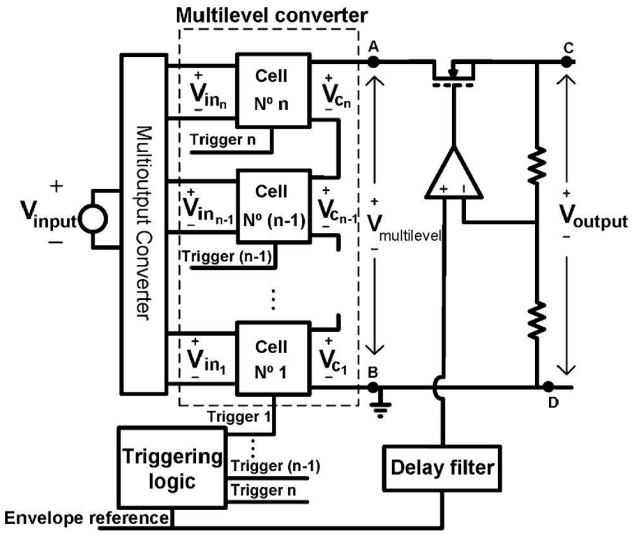


Fig. 4. Block diagram of the architecture with stacked cells for the envelope amplifier.

options need its own voltage sources. Therefore, an additional stage is necessary for the envelope amplifier. The final configuration (Fig. 4) is as follows.

- A first stage that supplies the multilevel converter that can be implemented with several single input—single output converters or with one single input—multiple output converter (e.g., multi-output flyback converter)
- The second stage is the multilevel converter that supplies the linear regulator. Two possibilities for its implementation are considered
- The third stage is the linear regulator, whose role is to regulate the desired envelope voltage

Main advantages of this three-stage series architecture for the envelope amplifier are:

- high bandwidth;
- high linearity;
- significantly higher efficiency compared to a linear regulator supplied by a constant voltage;
- negligible voltage ripple compared to a dc-dc converter solution obtained with a very low switching frequency.

There are several possibilities to implement the multilevel converter for this application:

- voltage cells stacked in series [23];
- multiplexed independent voltage sources [24].

Both solutions, the one shown in this paper and the solution presented in [23] are based on the architecture with voltage

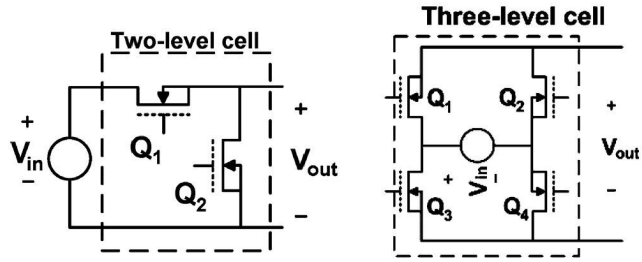


Fig. 5. Voltage cells that could be used as a solution to implement a multilevel converter.

cells stacked in series. The block diagram of the architecture with stacked cells, that consists of three-stages, can be seen in Fig. 4.

Additionally to the three main stages of the envelope amplifier, a triggering logic and a delay filter have to be included in the system, as seen in Fig. 4, to avoid a delay between the multilevel output voltage and the output voltage of the envelope amplifier.

The output voltage of the multilevel converter, Fig. 4, can be calculated as a combination of the output voltage of the cells:

$$v_{\mathbf{multilevel}} = \sum_{i=1}^{N} a_i V_{C_i} \tag{1}$$

where N is the total number of cells, $\mathbf{V_{Ci}}$ is the output voltage of the multilevel cells and $\mathbf{a_i}$ can take the following values:

- "+1": The input voltage of the cell is connected directly to the load;
- "0": The input voltage of the cell is not connected to the load, and 0 V are applied;
- "−1": The input voltage of the cell is connected inversely to the load.

Equation (1) applies for both design possibilities, two and three-level cells, but there are differences in the possible values of $\mathbf{a_i}$. In the case of two-level cell topology it is possible only to add voltages (only values "+1" and "0" of $\mathbf{a_i}$), while in the case of three-level cell topology it is possible to subtract as well ($\mathbf{a_i}$ can be "+1", "0" and "−1"). The negative voltage state of the three-level cell allows more voltage levels with the same number of cells, but also more power switches are needed, so in order to verify the potential advantages and the possible disadvantages of the three-level cell topology, a comparison with the two-level cell design has been carried out.

In the state of art, multilevel inverters that use a configuration with the three-level cell topology can be found. For this application, the multilevel converter with stacked three-level cells is the middle stage of an envelope amplifier that processes signals with always positive values.

For a better understanding of the operation of the three-level cell, Table I shows the cell's output voltage depending on the state of the cell's switches. It can be noticed that MOSFETs $\mathbf{Q_1}$ and $\mathbf{Q_2}$ (Fig. 5(right)) are complementary switches, as well as $\mathbf{Q_3}$ and $\mathbf{Q_4}$. Additionally, $\mathbf{Q_4}$ and $\mathbf{Q_2}$ are low-side MOSFETs, because their source is connected to the "ground" of the cells, while $\mathbf{Q_1}$ and $\mathbf{Q_3}$ are high-side MOSFETs.

TABLE I
OUTPUT VOLTAGE OF A THREE-LEVEL CELL DEPENDING ON THE STATE OF THE CELL'S POWER SWITCHES

Q_1	Q_2	Q_3	Q_4	V_{out}
ON	*OFF*	*OFF*	*ON*	V_{in}
OFF	*ON*	*ON*	*OFF*	$-V_{in}$
OFF	*ON*	*OFF*	*ON*	*0*
ON	*OFF*	*ON*	*OFF*	*0*

III. DESIGN CONSIDERATIONS FOR THE OPTIMIZATION OF THE NUMBER AND MAGNITUDE OF THE VOLTAGE LEVELS OF THE ENVELOPE AMPLIFIER

In this section, the number and magnitude of the voltage levels to optimize the design of the envelope amplifier is analyzed. The obtained optimized design will be used for the comparison (theoretical and experimental) between both types of cell topology of the multilevel converter.

The architecture of the multilevel converter improves the efficiency of the linear regulator stage compared to a constant voltage supply. However, two additional stages are needed to generate the variable high-bandwidth supply voltage with the drawbacks of a reduction in the efficiency and a complexity increase.

The number of voltage levels of the envelope amplifier, to improve the efficiency, the quality of the transmitted signal and the size of the converter, has to be established regarding the following design rules.

- Efficiency of the third stage: This is the most important factor, as the main advantage of the architecture is to reduce the losses in this stage
- Overall efficiency of the converter: more voltage levels implies better efficiency on the third stage but more power losses on the first and the second stage as a result of more cells and voltage input sources
- Simplicity: Complexity and size increase with the number of voltage levels
- Parasitic Components: As the number of levels rise, parasitic components of the layout, critical at high frequencies, become more important

To obtain an accurate model relating all this factors, some of them even difficult to quantify, is very complex. Hence, the determination of the optimum number of levels is complicated. However, it is feasible to calculate the improvement in the efficiency of the third stage. The first increments in the number of levels have a strong impact in the efficiency. For example, regarding the specifications of this work, described in Section IV, there is an improvement of 13% for a sinusoidal waveform and of 30% for a CDMA signal in the efficiency of the third stage as a consequence of increasing from one to three the number of voltage levels. This improvement becomes smaller for higher number of levels. For example, a transition from three to five voltage levels would imply improvements of 4% for a sinusoidal waveform and of 6% for a CDMA signal in the efficiency of the third stage. The procedure to obtain the theoretical efficiency improvements can be found in [25]. On the other hand, a high number of levels penalize the efficiency and simplicity of the first and second stages because more voltage sources and cells have to be added, increasing the losses for the same output power and also the size and complexity of the converter.

Hence, depending on the specifications (input voltage, characteristics of the transmitted signal, output power) the optimum number of levels must be determined regarding the complexity of the whole system and the efficiency improvement provided in the third stage by the considered number of levels.

Considering the specifications and a trade-off between the efficiency and the complexity, a system with three voltage levels has been designed. In [23] the optimization process for the calculation of the number and value of the voltage levels is explained in detail. The optimization to obtain the output voltages of the multilevel converter has been applied in the design of the envelope amplifier for each type of cell topology. The results of the optimization are the voltage levels of V_{MAX}, 3/4 V_{MAX} and 1/2 V_{MAX}, the same for both types of cell configuration for these specifications. The generation of the voltage levels depends on the type of voltage cell of the multilevel converter, as it is explained later.

IV. OPTIMIZED ENVELOPE AMPLIFIER DESIGN

Previous to the optimization of the envelope amplifier, the operation of each type of cell and the influence in the design of the system is analyzed. During this analysis it is assumed that the load is purely resistive, as it is the behavior of the non-linear power amplifier that it is supplied by the envelope amplifier inside the bandwidth of interest [26]. It is also analyzed at the end of the section the mean switching frequency of the multilevel converter for a real RF communication signal, which allows an estimation of the commutation losses of the multilevel converter. As explained at the end of the previous section, a configuration of three voltage levels has been selected for the comparison of both envelope amplifiers with the two types of voltage cells.

It can be seen that in the multilevel converter based on stacked voltage cells, there is always one cell that never changes its output voltage. This is because the linear regulator needs to have a minimum supply voltage in order to reproduce voltage levels higher than zero. In the case of the prototype with two-level cells, there is a voltage level equal to 0.5 V_{MAX} for a configuration of three voltage levels (as seen in previous section as a result of the optimization process for three voltage levels and these specifications), where V_{MAX} is the maximum voltage of the desired envelope. Later on, depending on the value of the envelope reference, the outputs of the voltage cells can be added to that constant voltage level. For the three-level topology design, the minimum voltage (0.5 V_{MAX} as well) is achieved by subtracting from the voltage source that is always connected to the load (3/4 V_{MAX}) the voltage sources of all the cells (one cell for the configuration with three voltage levels). At this point it is important to notice that the input source that never changes its output voltage does not need to be connected to a cell as it can be seen in Figs. 6 and 7. This implies the possibility to avoid isolation in that input voltage which leads to several advantages

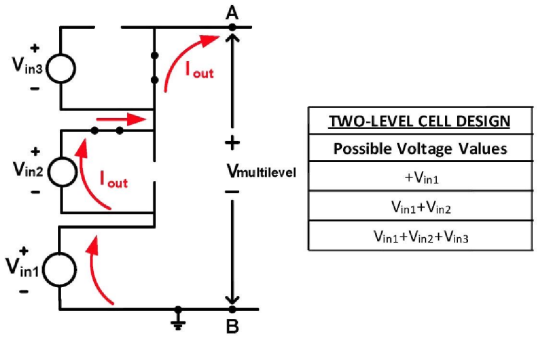


Fig. 6. Simplified schematic of a multilevel converter designed for three voltage levels configured to provide $Vin1 + Vin2$.

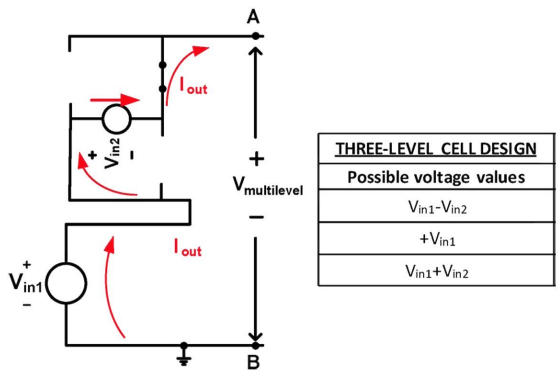


Fig. 7. Simplified schematic of a multilevel converter for a design with three voltage levels configured to provide $V_{in}1 - V_{in}2$.

in size, losses and weight compared to the implementation presented in [23] (and it is applicable to both types of cell configuration). In the next section, it is also presented an optimization in the design of the first stage based in the energy handled by each voltage input. This optimization can be used both to optimize the design of the first stage and to compare the design alternatives for the multilevel converter.

Firstly, for a better understanding, let us consider a multilevel converter designed with two-level cells, as it is shown in Fig. 6, where it is also included a table with the different values that can take the output voltage of the multilevel converter for the designed number of voltage levels.

It can be seen that the cells are supplied by three independent voltage sources, V_{in1}, V_{in2} and V_{in3} and that the output voltage is, in this example, equal to $V_{in1} + V_{in2}$. Therefore, when the high side MOSFET of the cell is turned on, the cell provides energy to the load, and when it is turned off, the cell's output is simply short-circuited.

The situation is a little bit different in the case of the three-level cells. In Fig. 7 a multilevel converter that employs one three-level cell is presented.

In this example two independent voltage sources, V_{in1} and V_{in2}, supply the employed voltage cells. In this configuration the voltage of the cell is equal to $-V_{in2}$. Therefore, the output of the multilevel converter is equal to $V_{in1} - V_{in2}$. It can be seen that the cell is connected inversely to the load. Depending on the probability density function of the amplitude, the mean power of each voltage source (at the low dynamic of the first stage) can be positive or negative. In the latter case, there will be reactive (or recirculation of) power that will be processed two times. Therefore, it is important to notice that depending on the state of the MOSFETs in the three-level cell, the cell's voltage source has to sink or to source the load current.

Consequently, the voltage source that supplies a three-level cell has to be bidirectional, which implies that topologies that are used to implement these voltage supplies must include synchronous rectification in order to sink and source the load current. This can be an advantage regarding the efficiency but it can be implemented also for the voltage sources of the two-level cell configuration so it has not been included in the comparison between both design alternatives.

As explained in the previous section, an envelope amplifier based on three-level cells has been implemented, with the same specifications of the envelope amplifier based in two-level cells. As a compromise between efficiency and complexity, it has been designed a system with three voltage levels as explained in Section II.

The specifications for the envelope amplifier are as follows:

- Input voltage of 24 V
- Variable output voltage from 0 V to 23 V
- The maximum instantaneous power is 50 W
- The maximum frequency of the reference signal is 2 MHz

For these specifications and based on the envelope amplifier with stacked cells, the optimization of the first stage (for both types of cells) based on the power share is presented, emphasizing on the differences between both design alternatives.

Analyzing the first stage of the architecture that utilizes the multilevel converter based on two-level and three-level cells, a huge difference can be easily noticed. As it is explained earlier, the first stage that supplies the three-level cells has to be bidirectional, although the load is purely resistive, and has one less output. This difference in the first stage in the case of two-level voltage cells is fundamental, because the flyback converter that is used to supply the two-level cell multilevel [23] converter cannot be used in this case. Therefore, it has been redesigned and, in order to guarantee the bidirectional flow of energy, a synchronous rectifier (SR) is considered. In the experimental prototype, a flyback with SR has been implemented.

Now, in order to optimize the design of the first stage, let us analyze the total energy supplied by each voltage level of the multilevel converter. First, let us assume that the signal that is amplified by the power amplifier has a density probability distribution of the signal's envelope like in Fig. 8.

Generally, for the signals with high PAPR, this distribution is a Rayleigh's distribution, but here it is approximated with a point-to-point linear function in order to simplify the calculations and it has not a strong influence in main conclusions. The data for the density distribution is taken from [27] for a CDMA signal.

The average power that should be supplied by the multilevel converter can be calculated as:

$$P_{\text{avg\_output}} = \frac{1}{R}\int_0^{V_{\max}} v_{\text{multilevel}}(v)p(v)vdv = 0.3097\frac{V_{\max}^2}{R} \quad (2)$$

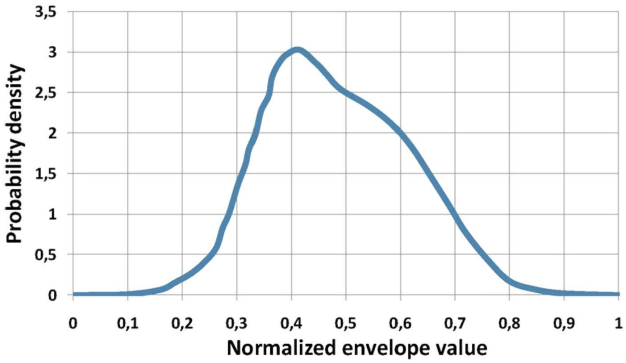


Fig. 8. Approximated Rayleigh's distribution for the envelope of a multicarrier signal.

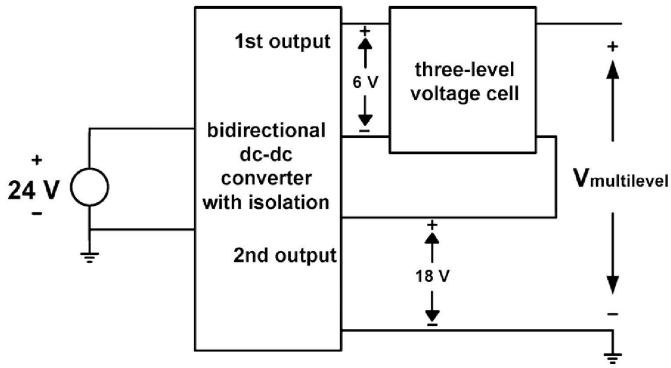


Fig. 9. Schematic block diagram of a multilevel converter implemented with a three-level voltage cell.

TABLE II
POWER SHARE HANDLED BY EACH VOLTAGE SOURCE WHEN THE RF ENVELOPE HAS A DISTRIBUTION LIKE IN FIG. 8 AND FOR A TWO-LEVEL CELL DESIGN

Cell	*Power share*
12 V cell	*77.3%*
First 6 V cell	*20.8%*
Second 6 V cell	*1.9%*

TABLE III
POWER SHARE HANDLED BY EACH VOLTAGE SOURCE IN THE CASE WHEN THE RF ENVELOPE HAS A DISTRIBUTION LIKE IN FIG. 8 AND FOR A THREE-LEVEL CELL DESIGN

Cell	*Power share*
18 V cell	*87.9%*
6 V cell	*12.1%*

In (2), V_{max} is the maximum level of the desired envelope, R is the equivalent load of the input impedance of the supplied non-linear power amplifier, $\rho(v)$ is the probability density function, $v_{multilevel}$ is the voltage at the output of the multilevel converter and v is the output voltage of the converter.

Let us consider two multilevel converters, one with two-level cells and the other with three-level cells. As said before and due to the optimization process there are two cells, for the design with two-level cells, each one supplied by a 6 V voltage source and there is a constant voltage level of 12 V that is always active. The three voltage outputs are generated by a single flyback converter from a source of 24 V. The average power supplied by each output of the flyback converter can be calculated given the amplitude probability density distribution (Fig. 8)

$$P_{\text{avg\_12 V}} = \frac{V_{\max}}{2R}\int_0^{V_{\max}} vp(v)dv = 0.2395\frac{V_{\max}^2}{R} \tag{3}$$

$$P_{\text{avg\_1st\_cell\_6 V}} = \frac{V_{\max}}{4R}\int_{0.5V_{\max}}^{V_{\max}} vp(v)dv = 0.0645\frac{V_{\max}^2}{R} \tag{4}$$

$$P_{\text{avg\_2nd\_cell\_6 V}} = \frac{V_{\max}}{4R}\int_{0.75V_{\max}}^{V_{\max}} vp(v)dv = 0.0057\frac{V_{\max}^2}{R} \tag{5}$$

It can be appreciated that $(3)+(4)+(5) = (2)$. All the terms of the equation are positives so the mean power supplied by each input source is positive.

Table II shows the power share of each voltage source that is used. As it can be seen, around 77% of the average power is supplied from the 12 V output.

To obtain the optimized voltage levels with three-level cells (the same voltage levels for this application), it is necessary to use an output of 18 V for the constant voltage level, and one 6 V output in order to reproduce 12 V and 24 V by subtraction or addition respectively. Fig. 9 shows the simplified block diagram of this solution.

The average power supplied by each output of the bidirectional single input multiple output converter would be (Table III)

$$P_{\text{avg\_18 V}} = \frac{3\,V_{\max}}{4R}\int_0^{V_{\max}} vp(v)dv = 0.3593\frac{V_{\max}^2}{R} \tag{6}$$

$$P_{\text{avg\_6 V}} = \frac{V_{\max}}{4R}\int_{0.75\,V_{\max}}^{V_{\max}} vp(v)dv - \frac{V_{\max}}{4R}\int_0^{0.5\,V_{\max}} vp(v)dv = -0.0496\frac{V_{\max}^2}{R} \tag{7}$$

It can be seen that the power supplied by the first output consists of two parts. The first integral of the (7) represents the power that the three-level cell provides to the load, and the second integral is the power absorbed by the cell.

It is obvious that all the power comes from the output that is used as a constant voltage (6), and that the three-level cell is actually used only to provide voltage levels that guarantee that there will not be distortion of the output signal, handling a low amount of average energy.

In this case, it is also complied that $(6)+(7) = (2)$ but in this case (7) is negative so (6) is higher than (2) and the input source of 6 V sinks current.

The input source that is always connected to the load, as explained before, does not need isolation, as seen in Figs. 6 and 7. The other input voltage sources will provide isolated outputs in order to supply the three-level voltage cells.

Having in mind that there are topologies with better efficiency than a flyback converter, and that the needed constant voltage level provides the major part of the output power, the first stage

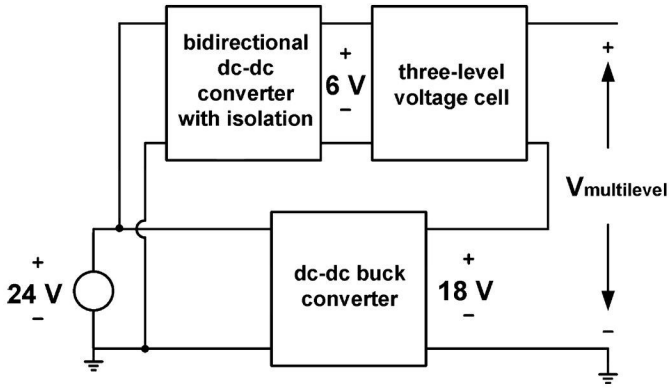


Fig. 10. Schematic block diagram of the multilevel converter implemented by combining a three-level voltage cell with a buck converter.

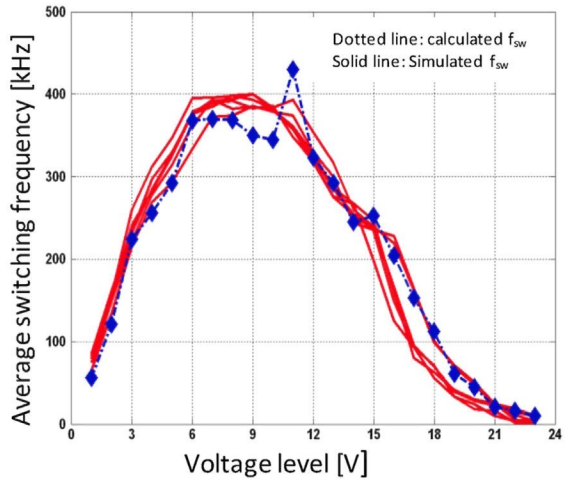


Fig. 11. Average switching frequency of the power switches of the multilevel cells as a function of the voltage level (calculated vs simulated).

can be divided into two sub-stages, as in Fig. 10. A simple high-efficiency buck converter can be used to produce the constant voltage level and a bidirectional flyback converter to supply the three-level cell like it is shown in Fig. 10, both connected to a single 24 V supply. This optimization, presented in this paper, can be done for the multilevel converter with both types of cell topology, but in the case of two-level cell topology and three voltage levels, an additional output for the flyback converter is necessary.

A solution like this could improve the overall efficiency, because the new flyback converter could be designed with an smaller transformer, the power losses connected to it could be decreased and the major part of the produced energy would be managed better through a buck converter with a higher efficiency than the flyback converter.

In this paper, the theoretical calculations are done for a sinusoidal signal and for a CDMA signal. For the sinusoidal signal, the multilevel converter has a switching frequency equal to the frequency of the transmitted signal. In a real RF communication signal the situation is different, so it is important to know the average switching frequency to estimate the commutation losses.

In Fig. 11 it is shown that the average switching frequency of the cells of the multilevel converter is significantly lower than the converter bandwidth (2 MHz). Therefore, the bandwidth of the proposed solution, in fact, is limited by the bandwidth of the linear regulator. The dotted blue line represents the calculated average switching and the solid red lines represent the simulated averaged switching frequencies for different voltage levels. The signals used to obtain the results shown in Fig. 11 are 64-QAM (quadrature amplitude modulation) signals.

V. Comparison of Two-Level and Three-Level Cells

In this section, the comparison of two-level cells and three-level cells is presented in terms of number of components, power losses, size, complexity and efficiency:

A. Number of Components

An important point of comparison between these two implementations of the multilevel converter is in the number of the voltage sources that are necessary to obtain a multilevel converter with N levels. If only two-level cells are used, N voltage sources are necessary to reproduce N voltage levels, and $2*(N-1)$ MOSFETs are used in total (two MOSFETs in each cell and the first voltage source connected directly to the load). On the other hand, when only three-level cells are used, approximately N/2 voltage sources are needed [1], and $2*(N-1)$ MOSFETs are employed in total (four MOSFETS in each cell). Regarding this point of comparison, a design with three-level cells has the same number of MOSFETs in the second stage and less input voltage sources for the multilevel converter that could lead to a less complicated first stage.

B. Power Losses Analysis

As it is explained in the previous paragraph, both solutions need the same amount of MOSFETs in order to reproduce N voltage levels, and always one-half of the employed MOSFETs conduct. Therefore, the conduction power losses are the same, and approximately can be estimated as

$$P_{\text{conduction}} = N R_{\text{ON}} I_{\text{RMS}}^2 \tag{8}$$

where N is the number of voltage levels produced by the multilevel converter, R_{ON} is the resistance of the employed MOSFETs and I_{RMS} is the effective current of the load. It is important to notice that the conduction losses increase with the number of implemented voltage levels, because there are more devices in series.

For both solutions, the maximum voltage that the MOSFETs inside the cell have to withstand is equal to the supply voltage of the cell and whenever there is a change of voltage level, the same number of MOSFETs is turned on/off in both types of cells. If the voltage levels are the same in both cases, and we use the same MOSFET drivers, the power losses due to parasitic capacitors in MOSFET's gate and between its drain and source should be, roughly, the same.

Therefore, we could expect more or less the same power losses in the multilevel converter (second stage) whether we implement it with two-level or with three-level cells. Also the linear regulator stage and the quality of the transmitted signal are the same for both alternatives of the multilevel converter.

C. Size and Complexity

An important difference is in the power supply that has to generate the voltage cells. For the same number of voltage levels of the multilevel converter, a design with the three-level topology alternative needs less number of cells. As a result of a lower number of cells, less voltage sources are needed, which leads to a simpler electrical and physical design. These advantages increase as the number of voltage levels (N) increases. For a higher N, more voltage sources are saved compared to the two-level cell solution. This implies fewer components and less size and losses in the first stage. As a conclusion, the design with three-level cells is a better design option to decrease the size and the complexity of the first stage of the envelope amplifier. These advantages increase with the number of voltage levels.

D. Efficiency

This field of comparison is the most important and the most complex to analyze due to the high number of parameters involved. The comparison has been done independently for each stage but main differences are found in the design of the first stage:

1) First Stage: As it is explained in Section A, for a three-level cell design less number of input sources are needed. It means that for the same output power, the first stage can have a higher efficiency as it is processed by less inputs.

The mean power handled by the input sources is an important factor because it affects highly to the efficiency and also because for the three-level cell design it can be negative. This would generate a circulating current that would decrease the efficiency. So the efficiency of this stage relies in the number of levels and in the mean power that supply each input source.

Another difference directly related to the efficiency of the envelope amplifier is the power share handled by the main input source (always connected to the load) of the envelope amplifier. For both types of design of the multilevel converter, this voltage source handles a higher percentage of the input power. As this voltage source does not need isolation, it can be designed to be a high efficiency optimized converter (a buck converter for example) to increase the overall efficiency.

Comparing both alternatives for the multilevel converter, the three-level cell main voltage source, of higher voltage due to the type of cell topology, handles more percentage of the power than the main voltage source of the design with two-level cells as it can be seen in Tables II and III, so higher efficiency can be expected. On the other hand, if the mean power of the input voltage source of a three-level cell is negative, there will be circulating power that it is processed two times, through the main voltage source and through the voltage source of the cell. As a conclusion, the best topology to implement the multilevel converter regarding this point of comparison will have to be chosen depending on the specifications (transmitted signal and output power). If the number of voltage levels is high, the three-level cell will be are more suitable option. For a smaller number of levels, it will have to be analyzed the maximum voltage of the envelope and the power share of the cell inputs to decide between both design alternatives.

2) Second Stage: The efficiency of this stage is roughly the same for both design alternatives, as the number of MOSFETs is the same and the voltages of the cells are the same or very similar.

3) Third Stage: The efficiency of the third stage is the same for both design options. The voltage levels will be chosen to obtain a high efficiency and will be the same of very similar with both design options. Main differences between both types of design can be found in the second and first stage.

E. Linearity and Bandwidth

As it is discussed in Section VII, both prototypes have the same characteristics of linearity and bandwidth so it can be concluded that there is not significant influence in the quality of the transmitted signal due to the implementation of the two or three-level cell multilevel converter.

Finally, the main points of comparison follow.

- The three-level cell topology design allows a first stage with less outputs, and therefore, with less components. The number of MOSFETs of the second stage for the same number of level is the same
- As a result of the lower number of voltage sources (less components and volume), the electrical and physical design is simpler for a three-level cell design.
- The power losses of the second (multilevel converter) and third (linear regulator) stage are very similar
- Regarding the efficiency of the first stage, the power share handled by the main input source is higher for the three-level cell multilevel converter design, but it can have recirculation of power if the mean power of the input voltage source of a cell is negative.
- As the number of voltage levels raises, the advantages of a design with three-level cells increase

As a conclusion, a simplification of the first stage can be achieved with the three-level cell and also an improvement in the efficiency of the first stage due to the power share and to the less components and inputs. However, under certain design specifications, the negative mean power of one or several inputs decreases the efficiency. To decide between both design alternatives, an analysis of all these factors must be done taking into account the probability density function of the transmitted signal and the main specifications (input voltage, maximum output voltage, output power and bandwidth).

VI. The Designed System

The implemented envelope amplifier based on the multilevel converter with three-level cells consists of three stages, detailed in Fig. 12.

The configuration of the three stages of the prototype is:

A. The First Stage: Single Input-Multiple Output Converter

In order to enhance the efficiency of the first stage, the constant voltage input source is produced by a synchronous buck converter that operates at a low switching frequency (50 kHz). The output filter is composed of four 68 μF capacitors made of tantalum and four ceramic capacitors of 100 nF and an inductor of 90 μH. The MOSFETs that are used are SI4886DY

First Stage: Synchronous buck converter and single-input single-output synchronous flyback	
V_{in}	24V
V_{out} buck	18V
V_{out} flyback (bidirectional)	6V
f_{SW} (buck and flyback)	50kHz
Peak output power	50W
Second Stage: Multilevel converter with one three-level cell of 6V	
Post Regulator: Linear Regulator	
Series element	MOSFET BLF177
Op. Amp.	LM6172

Fig. 12. Main implementation details of the three-stage envelope amplifier.

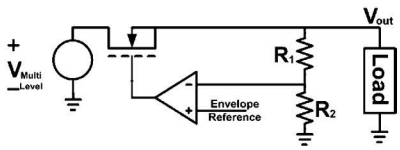


Fig. 13. Simplified schematic of the implemented linear regulator.

(the "floating" MOSFET) and BSH103. The transistors are selected regarding the estimated power losses and the maximum current and voltage that are specified.

Nevertheless, in the design of the synchronous bidirectional flyback converter, an additional circuit has been designed to obtain the control signals for the secondary high side MOSFET from the primary side control signal.

B. The Second Stage: Multilevel Converter Based on Three-Level Cells

The three-level voltage cells have been presented earlier. In order to understand how the cell should be controlled and implemented let us consider a three-level cell like in Fig. 5(right) and the control signals shown in Table I. The control of the power MOSFETs can be easily implemented using standard PWM drivers. One of the limitations is that the driver should be supplied by the voltage of the proper cell. This could be a problem if cell's supply voltage is low.

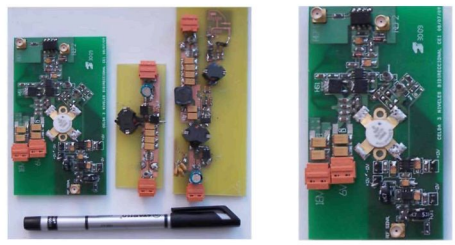
The second problem is that the control signals of the driver have to be referred to the "ground" of the voltage cell, and it is necessary to introduce isolation in order to apply the different control signals from the control ground to each cell ground.

The MOSFETs that are used in three-level cell are IRF3707Z and they are selected due to their low resistance and small parasitic components. The MOSFET drivers are LM27222. The selected drivers can be supplied with voltage levels as low as 4.5 V.

C. The Third Stage: Linear Regulator

The linear regulator is used as the post regulator, and it has to reproduce the reference signal. The schematic circuit of the linear regulator is shown in Fig. 13.

As it has been mentioned earlier, the bandwidth of the linear regulator is crucial for this design. Therefore, components that



(a) (b)

Fig. 14. Envelope amplifier based on the multilevel converter with three-level cells. On the right image: detail of the PCB with the second and the third stages.

can operate at high frequencies are used for the linear regulator's MOSFET and the operational amplifier. For the regulation of the linear regulator a wide bandwidth operational amplifier is selected. LM6172 bandwidth is 100 MHz in open loop [28]. The tests that we have conducted show that it can be supplied with asymmetric voltages. This is very important, because in order to drive the MOSFET used as a series element it is necessary to change its gate-source voltage from its threshold $(\mathbf{V_{th}})$ voltage to the value that is needed to conduct the maximum current of the envelope amplifier. The output voltage of the envelope amplifier changes from 0 V to 23 V, and this leads to the conclusion that the voltage applied to the gate of the MOSFET used as a series element should be, approximately, between 26 V and 27 V. In order to produce such a high voltage at its output, the positive voltage of the operational amplifier should be, at least, 28 V. Having in mind that the difference between the positive and negative supply voltage of the selected operational amplifier cannot be higher than 30 V, the selected supply voltages are 28 V and -2 V.

Criteria for the MOSFET selection are:

- the maximum drain-source voltage;
- thermal limits;
- MOSFET's input capacitance;
- MOSFET's transconductance.

Having in mind how the proposed system works, the maximum drain-source voltage of the MOSFET of this stage is equal to the maximum variation of the output voltage of the multilevel converter. The maximum current is equal to the quotient of the maximum voltage produced by the envelope amplifier and the input resistance of the supplied class E amplifier.

In order to obtain a wide bandwidth, the MOSFET's input capacitance should be as low as possible. Hence, the possible candidates for the MOSFET have been selected from HF/VHF power MOS transistors. The input capacitance of these transistors is in the order of hundreds of picofarads. Another advantage of having low input capacitance is in the control. It is controlled directly from the output of the operational amplifier and, therefore, the less input capacitance the better it is, because a high capacitance could lead to the current saturation of the operational amplifier's output.

High transconductance is important because it, actually, represents the voltage that should be applied between the MOSFET's gate and source. If the MOSFET has a low transconductance, it means that its gate voltage should be much higher than it is estimated (higher than 27 V). Several

MOSFETs from BLF series have been tested, and due to its good overall characteristics, BLF 177 has been selected.

An important characteristic of the envelope amplifier, specially for signals with high PAPR, is the maximum slew rate that it can provide. In this prototype, the slew rate of the envelope amplifier can be estimated using the data available in the technical documentation of the used components. It can be estimated from the maximum gate-current supplied by the operational amplifier LM6172 or by the maximum transconductance of the MOSFET BLF177, and the most restrictive of them will define the maximum slew rate of the envelope amplifier In this case is the first factor the one that limits the slew rate of the envelope amplifier. Using the information about the slew rate of the op.amp. LM6172 it has been obtained a slew rate equal to:

$$\begin{aligned} \text{Max. S.R.} &= \text{slew rate}_{\text{op.amp}} \\ &\quad \cdot \mathrm{R_{load}} \cdot \mathrm{g_m}/(1 + \mathrm{R_{load}} \cdot \mathrm{g_m}) \\ &= 2.95 \frac{\mathrm{kV}}{\mu\mathrm{s}} \end{aligned} \tag{9}$$

where $\text{slew rate}_{\text{op.amp}}$ is the theoretical maximum slew rate of the op. amplifier given in the datasheet, $\mathrm{R_{load}}$ is the load of the envelope amplifier (10 Ω) and $\mathrm{g_m}$ is the operational amplifier transconductance (6S). Equation (9) has been obtained by modeling the operational amplifier stage and calculating the output voltage as a function of the above referred parameters and the $\mathrm{V_{gate}}$ of the RF MOSFET.

However, the obtained value for the maximum slew rate considers a small signal parameter ($\mathrm{g_m}$) while the envelope signal has a large signal behavior. In order to provide a more accurate value, the data of the datasheet of the LM6172 amplifier and of the BLF177 transistor have been analyzed, and combining the maximum slew rate of the LM6172 (in a large signal test driving a capacitor similar to the input capacitor of the BLF177) with the BLF177 transconductance (Fig. 5 of the datasheet) the maximum slew rate is 800 V/μs. This value is considered high enough to cope with the specifications of a high-bandwidth communication signal.

VII. Experimental Results

The prototype for the validation of the theoretical results presented in this paper can be seen in Fig. 14. In Fig. 14(a) it can be seen three PCBs. In the right side it can be seen the bidirectional flyback. The buck converter is in the middle, and on the left side (green PCB) there are the multilevel and the linear regulator stages. In Fig. 14(b) it is shown a detail of the PCB with the second and third stages.

The prototype has been designed with independent modules except the critical stages (second and third), that deal with high frequency and high currents, which have been constructed on the same PCB to reduce the perturbations caused by the non-idealities of the layout.

In Fig. 14(a) it can be seen the reduced size of the magnetic components of the first stage compared with the solution presented in [23] for a two-level cells design for the same specifications, as a result of the first stage optimization presented in this work.

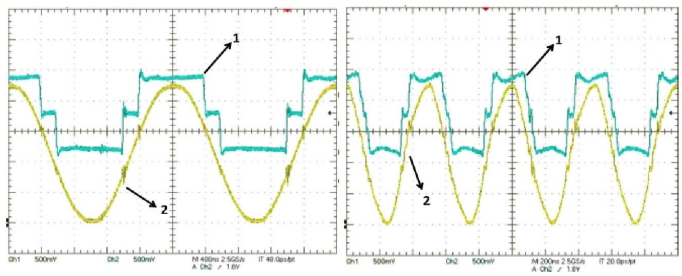


Fig. 15. Response of the multilevel converter (label 1) and envelope amplifier(label 2) when sine waves of 500 kHz(left; 400 ns/div) and 2 MHz (right; 200 ns/div) are used as the reference signal (5 V/div for all waveforms).

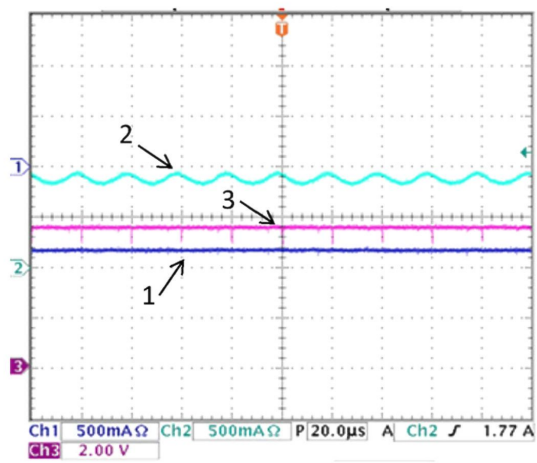


Fig. 16. Output voltage of the envelope amplifier (label 3), positive output current of the employed buck converter (label 2) and negative output current of the flyback converter that supplies the three-level voltage cell (label 1, the same DC value as label 2 but measured after the filter).

Fig. 15 shows the experimental waveforms of the response of the multilevel converter and the envelope amplifier when sine waves of 500 kHz and 2 MHz are used as the reference signal. The maximum output peak power for the test is 50 W for 23 V of maximum output voltage.

It has been explained earlier that the voltage source of the three-level cell has to be bidirectional. The need for the bidirectional source can be seen in Fig. 16. In the point of operation shown in the oscilloscope, the output voltage of the envelope amplifier is lower than 12 V and the buck converter has to supply current and flyback converter to sink it. It can be seen that the measured output currents of these two converters are equal (800 mA), but with different direction.

Firstly, the efficiency measurements of the first stage, which consists of the employed buck and the bidirectional flyback converter, are presented. Fig. 17 shows the measured efficiency of the buck converter and it can be seen that it is higher than 95% in very wide range of output power.

The measured efficiency of the bidirectional flyback converter that supplies three-level voltage cell is shown in Fig. 18. As it is expected, the efficiency of the flyback converter is lower than the efficiency of the buck converter and its maximum value is around 90%.

Comparing both efficiencies it can be seen the importance in the overall system efficiency of the percentage of power that each voltage source handles.

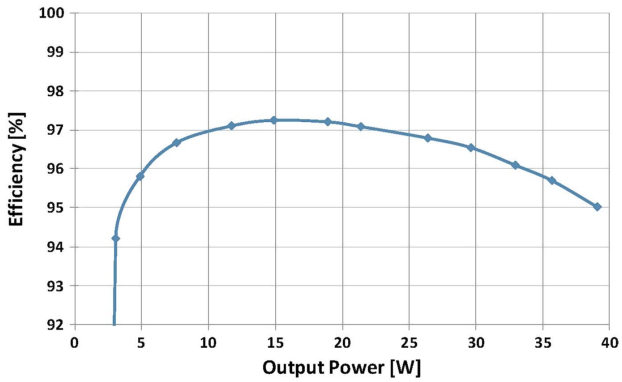


Fig. 17. Measured efficiency of the buck converter that is used in the first stage of the prototype with three-level cells.

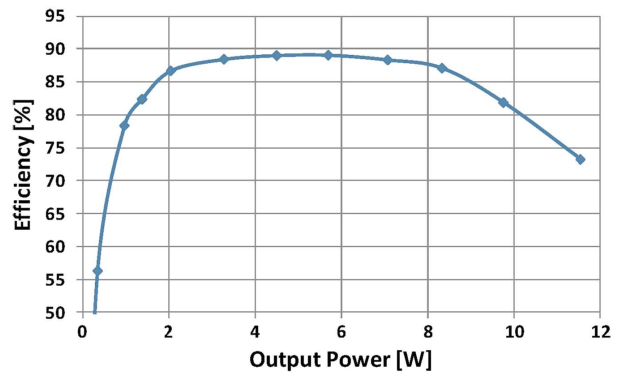


Fig. 18. Measured efficiency of the bidirectional flyback converter that is used in the first stage of the prototype with three-level cells.

TABLE IV
COMPARISON OF THE MEASURED EFFICIENCY OF THE THREE-LEVEL CELL ENVELOPE AMPLIFIER WITH OTHER DESIGN ALTERNATIVES FOR A 2 MHZ SINE WAVE

Vsin (V)	*Three Level Cell [this work]*	*Two Level Cell [23]*	*Ideal Regulator supplied with 23V*
0-9	46.7%	42.8%	29.3%
5-14	52.7%	56.0%	45.9%
0-22.5	63.2%	69.3%	73.4%

The efficiency of the envelope amplifier is measured for sine waves of different amplitudes on the three-level prototype and compared to the measurements of the prototype based on two-level cells [23] and also to the theoretical efficiency of an ideal linear regulator supplied with 23 V. The load of the envelope amplifier is a 10 Ohm resistor. The results are shown in Table IV. In Table V are shown the measured power losses of the three-level cell prototype obtained in this work in the same operating conditions than the results of Table IV. As in a two-level cell design, the efficiency of the implemented envelope amplifier depends on the average value of the reproduced sine wave, its frequency and amplitude.

The efficiency of the implemented envelope amplifier is significantly higher (up to 18%) than the efficiency of an ideal linear regulator supplied by a constant voltage when sine wave envelopes that have low average value are transmitted (sine wave from 0 V to 9 V, output power is around 3 W). This leads to

TABLE V
MEASURED POWER LOSSES OF THE THREE-LEVEL CELL PROTOTYPE FOR DIFFERENT SINE WAVES OF 2 MHZ [THIS WORK]

Vsin(V)	*Measured input power [W]*	*Measured output power [W]*	*Measured total power losses [W]*
0-9	*6.0*	*2.8*	*3.2*
5-14	*17.3*	*9.1*	*8.2*
0-22.5	*27.2*	*17.2*	*10.0*

TABLE VI
MEASURED POWER LOSSES OF THE TWO AND THREE-LEVEL CELL PROTOTYPE FOR DIFFERENT SINE WAVES OF 500 KHZ AND 2 MHZ

Vsin (V)	*Frequency of the sine wave (MHz)*	*Measured efficiency of the three-level cell prototype [this work]*	*Measured efficiency of the two-level cell prototype [23]*	*Theoretical efficiency of an ideal linear regulator supplied by the multilevel converter*
0-9	*0.5*	*45.9%*	*42.3%*	*56.3%*
5-14	*0.5*	*58.6%*	*58.7%*	*72.2%*
0-22.5	*0.5*	*71.3%*	*70.6%*	*86.4%*
0-9	*2*	*46.7%*	*42.8%*	*56.3%*
5-14	*2*	*52.7%*	*56.0%*	*72.2%*
0-22.5	*2*	*63.2%*	*69.3%*	*86.4%*

50% lower power losses (power savings of 3.2 W) and demonstrates great benefit of this solution when the signals with high PAPR are transmitted.

There are two major reasons for the significant difference between the measured efficiency of the envelope amplifier and the efficiency of an ideal linear regulator supplied by a multilevel converter (for a 2 MHz sine wave the efficiencies in the latter, shown in Table VI, are 56.3%, 72.2% and 86.4% for the three types of sine waves measured from the smaller to the bigger one). The first reason is the efficiency of the buck converter, flyback converter and the multilevel converter that are used to produce the desired voltage levels. For the estimation it is assumed that the efficiency of the first and the second stage is ideal, without losses. The second reason for the difference is that when the efficiency of the linear regulator is calculated it is assumed that the voltage levels are switched ideally with infinite speed and that the series element can have the minimum voltage drop of zero volts. Unfortunately, the voltage levels have to be triggered sufficiently before the theoretical value, in order to guarantee that there will not be any distortion at the output, and the minimum voltage drop at the series element is approximately 1 V. Due to all these reasons there is a significant difference between the estimated and measured efficiency.

For the sine waves of small and medium average values the prototype based on three-level voltage cells has slightly higher efficiency than the prototype that employs two-level cells and it is mainly due to the higher efficiency of the first stage, which has been improved applying the conclusions obtained on the studies of the energy handled by the input voltage sources.

Due to the higher parasitic inductances of the PCB, the efficiency of the three-level cell based prototype (less optimized) is lower when it is necessary to use all voltage levels (0 V–22.5 V) and these differences gain on importance if high frequency signals have to be reproduced. For three and two-level cell prototypes the efficiency drops from 71.3% and 70.6% to 63.2% and

69.3% respectively when the frequency of the signal changes from 500 kHz to 2 MHz, as shown in Tables IV and VI.

On both prototypes, for sine waves that need two or three voltage levels active, the power losses change depending on the frequency of the signal. This is due to the switching losses of the MOSFETs that are used in three-level cell. When the reproduced sine wave is below 12 V there are not switching losses, because there is only one active voltage level, so the efficiency does not decrease at higher frequencies.

The efficiency of the prototype with three-level cells is better than the efficiency of an ideal linear regulator even when it is necessary to use two voltage levels. Unfortunately, when the envelope has an excursion from its minimum to its maximum (not the common situation as the transmitted signals have high PAPR), the efficiency of the prototype is lower than in the case of an ideal linear regulator. It can be seen in Table VI that it falls for 71,3% to 63,2% due to change of sine wave from 500 kHz to 2 MHz. Like in the case of the prototype that employs two-level voltage cells, the reason for that are high switching losses.

The efficiency results shown in this work correspond to the envelope amplifier. The overall power amplifier efficiency results are 35% and 41% for 43.8 dBm and 24.3 dBm of output power respectively for different sine waves as shown in [29] and 43% for a 64QAM modulation [30] and 13 W of output power, using a 125 MHz carrier on both cases.

In [31] it is shown that the bandwidth of the envelope amplifier is very important to achieve high linearity of the Kahn's transmitter. To obtain high linearity, the bandwidth of the envelope amplifier should be, at least, twice the bandwidth of the reference signal. In order to determine the bandwidth of the envelope amplifier two tests have been conducted. The first one is to apply a sine wave of the maximum amplitude as the envelope reference and to measure the response of the envelope amplifier.

In this way, it has been shown that the bandwidth of the implemented envelope amplifier is, at least, equal to the bandwidth of the signal that will be used as the reference. When the frequency of the reference sine wave of the maximum amplitude is increased over 2 MHz, the multilevel converter cannot respond so rapidly, and the output of the envelope amplifier is distorted. However, this does not mean that the implemented envelope amplifier cannot reproduce higher harmonics. The higher harmonics that are very important for high linearity of Kahn's transmitter usually are of much smaller amplitudes than the maximum amplitude that can be reproduced by the envelope amplifier. As long as the average switching frequency of employed MOSFETs does not exceed the bandwidth of the envelope signal (2 MHz in our case), the envelope amplifier reproduces the envelope reference correctly. For example, if the reference signal is a rectified sine wave of frequency f, its spectrum is infinite and consists of tones that are placed at frequencies $2f, 4f, 6f \ldots$ A rectified 500 kHz sine wave of the maximum amplitude is used as the reference and the response of the envelope amplifier is measured.

Fig. 19 shows the spectrum of the reference and of the output signal. It can be seen that up to 5 MHz all the spectral components are reproduced correctly.

Having in mind the theoretical analysis in [31] and the measurements presented in this chapter, it can be concluded that

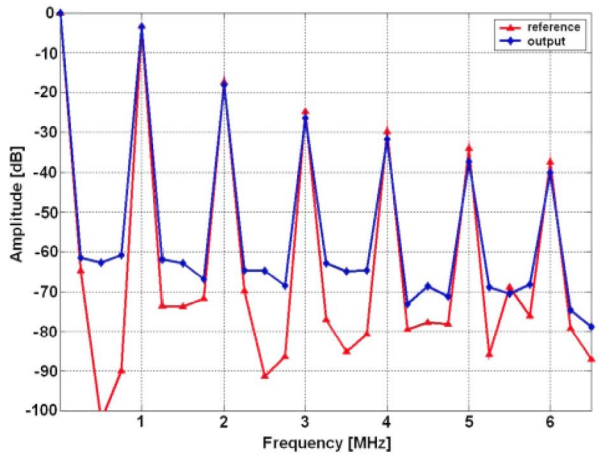


Fig. 19. Spectrum of the reference and output signal when a rectified 500 kHz sine wave is used as the reference. All the values are scaled to the dc value of the signal.

Kahn's transmitter that uses this envelope amplifier can achieve a linearity of 30 dB for the RF signals with a bandwidth of 5 MHz.

The high linearity of the envelope amplifier is needed to avoid additional spectral components in the spectrum of the applied output signal. In order to measure the linearity of an amplifier it is necessary to use a two-tone signal as a reference and to analyze the spectrum of the output [32]. If the two tones have frequencies of f1 and f2, the linearity is measured in dBs and it is represented as follows:

$$\text{Linearity} = 20\log\left(\frac{V(f_1)}{V(2f_1 - f_2)}\right) \tag{10}$$

where $\mathbf{V(f_1)}$ and $\mathbf{V(2f_1 - f_2)}$ are spectral components of the output signal at $\mathbf{f_1}$ and $\mathbf{2f_1 - f_2}$ respectively.

The results of the linearity measurements can be seen in Fig. 20. The frequency sweep has been done from 10 kHz to 2 MHz with constant distance of 50 kHz between the two tones. The response of the envelope amplifier has been measured in an oscilloscope and the measured data are later processed in MATLAB. The obtained attenuation of the third order intermodulation products is around 50 dB, which is in the range of interest.

VIII. Conclusion

In this paper, a multilevel converter, based on a three-level cell, is analyzed and compared with an existing solution, the two-level cell topology. Several advantages of the three-level cell design are presented, analyzed and experimentally tested. Both solutions have a 2 MHz bandwidth and provide up to 50 W of instantaneous power.

A comparison between both possibilities for the multilevel converter from the point of view of the simplicity of the design, the number of inputs and efficiency is carried out. It has been demonstrated that in the case of the solution with three-level cells the first stage of the envelope amplifier can be smaller (due to less number of voltage sources that supply the multilevel converter), but the first stage has to be bidirectional. The second stage for both design alternatives have roughly the same power

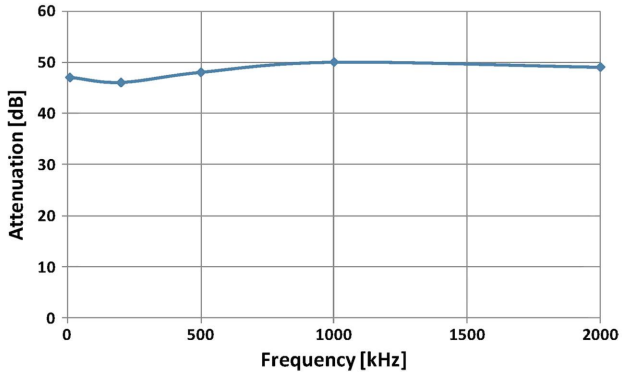


Fig. 20. Attenuation of the intermodulation products when two tone signals are used as the reference for the envelope amplifier (the distance between the two tones, 50 kHz, is maintained constant during the test).

losses, but with a three-level cell design the reference can be followed more accurately. On the other side, three-level cells are bigger than two-level cells, being the number of MOSFETs the same for both design alternatives.

As the number of voltage levels increase, the solution with three-level cells has more advantages over the two-level cell design due to the less voltage sources. This implies less volume and size and therefore, less complexity of the solution to achieve the same number of voltage levels.

For an envelope with small and medium average values the prototype based on three-level voltage cells has slightly higher efficiency than the prototype that employs two-level voltage cells and it is mainly due to the higher efficiency of the first stage.

Analyzing the energy handled by the first stage inputs of each multilevel configuration (two or three-level topology), it has been shown that a multilevel designed with three-level cells can achieve a higher efficiency on the first stage. On the other hand, this advantage in the first stage efficiency can be lost if any of the input sources has negative mean power because of the recirculation of current.

The efficiency of both envelope amplifiers has been measured for different sine waves. When the sine waves have low and medium average value, which is the most common situation, both solutions are significantly better than a linear regulator supplied by constant voltage. In the case that the envelope signal is a sine wave ranging from 0 V to 9 V (output power is around 3 W), the hybrid solution presented in this paper has up to 50% lower power losses than the classical linear regulator, while in the case of sine wave between 5 V and 14 V the power losses are lower by 39%.

The linearity of the prototype is measured as well and the attenuation of the intermodulation products is around 50 dB for the frequency range of interest, and ensures the quality of the transmitted signal.

REFERENCES

[1] D. Diaz, M. Vasić, O. Garcia, J. A. Oliver, P. Alou, and J. A. Cobos, "Comparison of two different cell topologies for a multilevel power supply to achieve high efficiency envelope amplifier," in *Proc. IEEE ECCE'09*, Sep. 2009, pp. 25–30.

[2] S. Roy, "Energy logic for telecommunications," *White Paper for Emerson Network Power*, Sep. 2008.

[3] G. Pierre, "Power system efficiency in wireless communication," in *Special Presentations, APEC*, 2006.

[4] S. Whittle, "The RF Sting in the Digital Transmission Tail," 2010.

[5] N. D. Lopez, X. Jiang, D. Maksimovic, and Z. Popovic, "A high-efficiency linear polar transmitter for EDGE," in *IEEE Radio Wireless Symp. Dig.*, Jan. 2008, pp. 199–202.

[6] D. Kim, D. Kang, J. Choi, J. Kim, Y. Cho, and B. Kim, "Optimization for envelope shaped operation of envelope tracking power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 5, pp. 1787–1795, May 2011.

[7] M. Hoyerby and M. Andersen, "TEDS base-station power amplifier using low-noise envelope tracking power supply," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 7, pp. 1687–1693, Jul. 2009.

[8] J. Kim, B. Fehri, S. Boumaiza, and J. Wood, "Power efficiency and linearity enhancement using optimized asymmetrical Doherty power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 2, pp. 425–434, Nov. 2010.

[9] M.-W. Lee, S.-H. Kam, Y.-S. lee, and Y.-H. Jeong, "Design of highly efficient three-stage inverted Doherty power amplifier," *IEEE Microw. Wireless Components Lett.*, vol. 21, no. 7, pp. 383–385, Jun. 2011.

[10] J. Moon, J. Kim, J. Kim, I. Kim, and B. Kim, "Efficiency enhancement of Doherty amplifier through mitigation of the knee voltage effect," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 1, pp. 143–152, 2011.

[11] L. R. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proc. IRE*, vol. 40, no. 7, pp. 803–806, Jul. 1952.

[12] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.

[13] P. Midya, K. Haddad, L. Connell, S. Bergstedt, and B. Roeckner, "Tracking power converter for supply modulation of RF power amplifiers," in *Proc. IEEE PESC*, 2001, vol. 3, pp. 1540–1545.

[14] J. Staudinger, B. Gilsdorf, D. Newman, G. Norris, G. Sadowniczak, R. Sherman, and T. Quach, "High efficiency CDMA RF power amplifier using dynamic envelope tracking technique," in *Proc. Int. IEEE MTT-S*, Jun. 2000, vol. 2, pp. 873–876.

[15] A. Soto, J. A. Oliver, J. A. Cobos, J. Cezon, and F. Arevalo, "Power supply for a radio transmitter with modulated supply voltage," in *Proc. Appl. Power Electron. Conf. APEC'04*, Feb. 2004, vol. 1, pp. 392–398.

[16] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking in RF power amplifiers," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 549–552, Mar. 2006.

[17] "Method and Apparatus for High Efficiency Wideband Power Amplification," U.S. Patent 6 084 468, Jul. 2000.

[18] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Efficiency optimization in linear assisted switching power converters for envelope tracking in RF power amplifiers," in *Proc. IEEE ISCAS*, May 23–26, 2005, vol. 2, pp. 1302–1305.

[19] F. H. Raab, B. E. Sigmon, R. G. Myers, and R. M. Jackson, "L-band transmitter using Kahn EER technique," *IEEE Trans. Microw. Theories Tech.*, vol. 46, no. 12, pt. 2, pp. 2220–2225, Dec. 1998.

[20] V. Pinon, F. Hasbani, A. Giry, D. Pache, and C. Gamier, "A single-chip WCDMA envelope reconstruction LDMOS PA with 130 MHz switched-mode power supply," in *Proc. ISSCC*, Feb. 3–7, 2008, pp. 564–636.

[21] L. Marco, E. Alarcon, and D. Maksimovic, "Effects of switching power converter nonidealities in envelope elimination and restoration technique," in *Proc. ISCAS*, May 21–24, 2006, pp. 3137–3140.

[22] M. Hoyerby and M. Andersen, "Ultrafast tracking power supply with fourth-order output filter and fixed-frequency hysteretic control," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2387–2398, May 2008.

[23] M. Vasić, O. Garcia, J. A. Olilver, P. Alou, D. Diaz, and J. A. Cobos, "Multilevel power supply for high efficiency RF amplifiers," in *Proc. 24th IEEE APEC*, Washington, USA, Feb. 2009, pp. 1233–1238.

[24] M. Vasić, O. Garcia, J. A. Oliver, P. Alou, D. Diaz, and J. A. Cobos, "Switching capacities based envelope amplifier for high efficiency RF amplifiers," in *Proc. 25th IEEE APEC*, Palm Springs, Feb. 2010, pp. 723–728.

[25] M. Vasic, "Wide Bandwidth High Efficiency Power Converter for RF Amplifiers," Ph.D. dissertation, Universidad Politécnica de Madrid, Madrid, Spain, 2010.

[26] F. Raab, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. 24, no. 12, pp. 725–735, Dec. 1977.

[27] V. Yousefzadeh, "Digitally Controlled Power Converters for RF Power Amplifiers," Ph.D. dissertation, Univ. Colorado, Boulder, Aug. 2006.

[28] Datasheet of LM6172, National Semiconductor. May, 1999.
[29] M. Vasic, O. Garcia, J. A. Oliver, P. Alou, D. Diaz, J. A. Cobos, A. Gimeno, J. M. Pardo, C. Benavente, and F. J. Ortega, "High efficiency power amplifier for high frequency radio transmitters," in *Proc. APEC*, Feb. 21–25, 2010, pp. 729–736.
[30] M. Vasić, O. Garcí, J. A. Oliver, P. Alou, D. Diaz, J. A. Cobos, A. Gimeno, J. M. Pardo, C. Benavente, and F. J. Ortega, "High efficiency power amplifier based on envelope elimination and restoration technique," *Proc. ECCE*, pp. 3833–3840, Sep. 12–16, 2010, vol., no..
[31] F. H. Raab, "Intermodulation distortion in Kahn-technique transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 12, pp. 2273–2278, Dec. 1996.
[32] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "RF and microwave power amplifier and transmitter technologies Part 1," *High Frequency Magazine*, pp. 22–36, May 2003.

Daniel Díaz was born in Madrid, Spain, in 1980. He received the M.Sc. degree in industrial electronics from the Universidad Politécnica de Madrid, Spain, in 2009, where he is currently pursuing the Ph.D. degree in electrical engineering.

His research interests include modeling and control of switched power supplies, RF circuits design and digital control for power converters.

Miroslav Vasić was born in Serbia 1981. He received the M.S. degree from the University of Belgrade, School of Electrical Engineering, Serbia, in 2005. He received the M.S. and Ph.D. degree in industrial electronics from the University of Madrid, Spain, in 2008 and 2010, respectively.

Since 2010, he has been working as a Researcher in Centro de Electronica Industrial (CEI), Madrid. His research interests include switching mode power supplies, RF circuit design and digital control applied to power electronics.

Oscar García (M'99) was born in Madrid, Spain, in 1968.

He is a Full Professor at Universidad Politecnica de Madrid. He has been involved in more than 70 research projects, holds 8 patents and he has published more than 150 technical papers in conferences and journals. He is vice-president of the Center for Industrial Electronics (CEI-UPM).

Prof. Garcia received the UPM Research and Development Award for faculty less than 35 years in year 2003 and the UPM Innovation in Education Award in year 2005.

Jesús Á. Oliver (M'00) received the M.S. and Ph.D. degrees in electrical engineering from Universidad Politécnica de Madrid, Madrid, Spain, in 1996 and 2007, respectively.

In 1996, he was a Visiting Scholar at CPES, and in 2000 he held a summer internship at GE R&D, Schenectady, NY. Since 2001, he has been an Assistant Professor of electrical engineering at Universidad Politécnica de Madrid, and in 2007 he became Associate Professor. He has published over 100 technical papers and holds three patents. He has been actively involved in over 60 R&D projects for companies in Europe, the U.S., and Australia. His research activities include modeling and control of power electronics converters and systems, high dynamic response power converters for RF applications and energy efficient applications.

Pedro Alou (M'07) was born in Madrid, Spain, in 1970. He received the M.S. and Ph.D. degrees in electrical engineering from the Universidad Politécnica de Madrid (UPM), Spain, in 1995 and 2004, respectively.

He is has been Professor of UPM since 1997. He has been involved in power electronics since 1995, participating in more than 40 R&D projects with the industry. He has authored or coauthored over 100 technical papers and holds three patents. Main research interests are in power supply systems, advanced topologies for efficient energy conversion, modeling of power converters, advanced control techniques for high dynamic response, energy management and new semiconductor technologies for power electronics. His research activity is distributed among industrial, aerospace and military projects.

Roberto Prieto (M'99) has been an Associate Professor at the Technical University of Madrid (UPM), Spain, in the Power Electronics Group (División de Ingeniería Electrónica—DIE) since 1998.

Since 1999, he has been coordinating the Modeling and Computer Aided Design Division of the Power Electronics Research Group. Prior to that, he was an Assistant Professor in the same group for five years (1993). He has published more than 120 papers at international conferences (most of which were sponsored by IEEE). He is also a coauthor of three international patents and a technical advisor for several IEEE conferences and journals. He has been the advisor on more than 20 master's theses and 5 doctoral theses and has participated in more than 60 research projects. His main research interest is the design and modeling of magnetic components and power electronics systems.

José A. Cobos received the M.S. and Ph.D. degrees in electrical engineering from the Technical University of Madrid (UPM), Spain, in 1989 and 1994, respectively.

He has been a Professor at UPM since 2001. His contributions are focused in the field of power supply systems for telecom, aerospace, industrial, automotive and medical applications. His research interests include energy efficiency in microprocessors and RF amplifiers, magnetic components, piezoelectric transformers, transcutaneous energy transfer and dynamic power management. He advised 12 Doctoral dissertations. He published over 200 technical papers and holds 6 patents. He is the Director of the "Centro de Electrónica Industrial, CEI-UPM", a university research center, leading a strong industrial program in power electronics, with technology transfer through more than 50 direct R&D contracts with companies in Europe, U.S., Australia and China.

Prof. Cobos received the "UPM Research and Development Award for faculty less than 35 years of age," and the "Richard Bass Outstanding Young Power Electronics Award of the IEEE" (in 2000). The CEI-UPM was awarded among the top 5 European universities by the EPSMA in 2007, and awarded with the "UPM Technology transfer award" in 2006. For many years he has been cooperating with the IEEE and other professional associations. He was AdCom member of the IEEE Power Electronics Society (PELS) from 2001 to 2006 as Chair of the Technical Committee on DC Power Supply Systems.